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Behaviour of SOI MOSFET in Nano Regime

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Abstract— **Continuous technology scaling in device dimension give rise to short channel effects which are of major concerned in nano regime and need to be addressed in future VLSI generation . Silicon-on-insulator (SO I) MOSFET in this decade has been offering superiority over CMOS devices with higher speed, higher density, excellent radiation hardness and reduced short channel effects for submicron VLSI applications. The SO I based MO SFETs present a definitive advantage in the highly competitive domain of Low Power/Low Voltage (LP/LV) electronics circuits. In this work the effect of channel doping variations on the behaviour of nano scale SO I based MO SFET has been examined. Variations in doping concentration of SO I MO SFET channel is explored to study the impact of channel doping on short channel effects (SCEs) such as threshold voltage fluctuation, subthreshold swing (SS), gate leakage, I_{on} current, I_{off} current and drain induced barrier l owering (DIBL) of N- channel SO I MOSFET. TCAD Simulation has been used in this work .**

Keywords—**silicon on insulator (SO I) film, density gradient (DG) transport model, buried oxide (BO X), subthreshold slope (SS), drain induced barrier lowering (DIBL).**

I. Introduction

To achieve density, speed and power optimization the dimensions of the device has been shrinking down for the last three decades . So it is not easy to continue with bulk MOSFET because of short channel effects problem in sub < 100nm regime. Short channel effects are less dominant on SOI based MOSFETs than their BULK counterpart. But still SOI based MOS devices are suffering to a less extent with short channel effects such as gate leakage and subthreshold leakage due to continuous scaling of threshold voltage and supply voltage in nanogeneration. So to optimize the SOI devices channel doping optimization is one of the option to control short channel effects (SCEs) and performance improvement. DIBL causes shift in threshold voltage in linear (V_{DS}=0.05V) and saturation (V_{DS}=V_{DD}) region results in lowering the barrier of a short-channel device which in turn increases the subthreshold current . SOI has more speed than bulk MOSFETs due to reduced capacitance and provide better isolation due to buried oxide layer (BOX) thereby makes charge leakage impossible. Small capacitance makes SOI devices attractive for low power, low voltage application and accepted as better option for gate length <25nm in nano regime. SOI Devices provide high packing density also but yet they are suffering from self heating effect and floating body effect. In this paper, we will elaborate the effect of channel doping variations in a 50nm technology N-channel fully depleted SOI MOSFET.

II. Design Method

A metal gate technology based fully depleted n-channel SOI MOSFET has been designed using TCAD Sentaurus Structure Editor. The tecplot architecture of n-channel fully depleted silicon on insulator MOSFET is shown in Fig. 1. The active elements are formed in active silicon layer (SOI film) region which is separated from the substrate by using a buried oxide layer (BOX) made of SiO_2. The material SiO_2 is also used for making gate oxide and spacer technology to reduce fringing field effect. The carrier transport model used for all simulation is Density Gradient (DG) includes carrier mobility degradation due to high doping concentration, the velocity saturation within high-field regions and the mobility degradation due to surface roughness scattering.

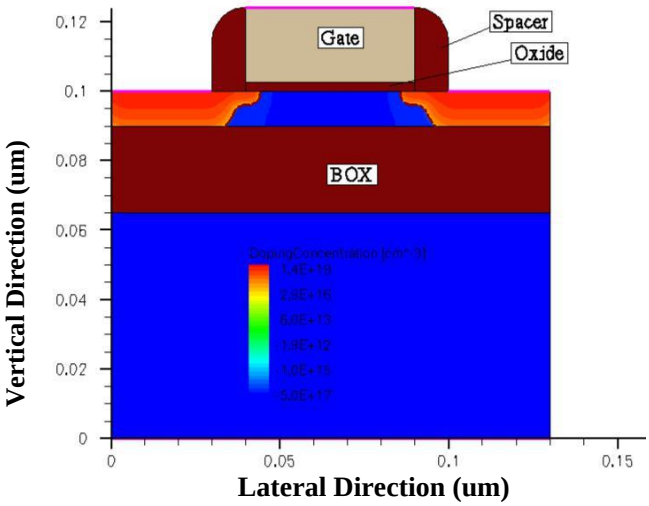

Fig. 1 FDSOI NMOSFET with Channel Doping $5x10^{17}$ cm^{-2}

TABLE I
DEVICE PARAMETERS T AKEN FOR DESIGN

S .No.	Parameter	Value [unit]
1.	Gate Length	50 [nm]
2.	Gate oxide thickness	2.5 [nm]
3.	BOX thickness	25 [nm]
4.	Spacer thickness	10 [nm] each side
5.	SOI film thickness	10 [nm]
6.	Substrate Doping	5 x 10^{17} [cm^{-2}]
7.	Lateral diffusion (L_D)	5[nm] each side

The DG model solves the quantum potential equations to include quantization effects in a classical device simulation. In the density-gradient transport approximation the quantum potential is a function of the carrier densities and their gradients. The nanoscale devices, such as double gate SOI and FinFETs structures are also simulated with the help of Sentaurus Simulator. The dimensions and doping information regarding to Design of NMOS Structure is given in table I.

III. RESULTS

The behaviour n-channel SOI MOSFET in nano regime has been characterized with different channel doping concentration with value N_{ch} = 1x10^{17}, 2.5x10^{17} , 5x10^{17}, 7.5x10^{17} and 1x10^{18} cm^{-2} . Fig. 2 shows the threshold voltage versus channel doping concentration. It is appearing from the graph, threshold voltage almost linearly depends on channel doping concentration. From this we observed that control on short channel effects become worse at channel doping concentration less than 1x$10^{17}$$cm^{-2}$ for 40nm channel length SOI NMOSFET. The values of I_{on} and I_{off} current at various channel doping concentration is given in table II. The effect of channel doping variation on I_{on} of the MOSFET is shown in Fig. 3. Since the threshold voltage increases due to increase in channel doping results in decrease in I_{on} current of the device. Similarly effect on off state current (I_{off}) with channel doping concentration is shown in Fig. 4. It is clear from the graph, relation between Logarithmic of off state current ($\log_e I_{off}$) and channel doping concentration is almost linear.

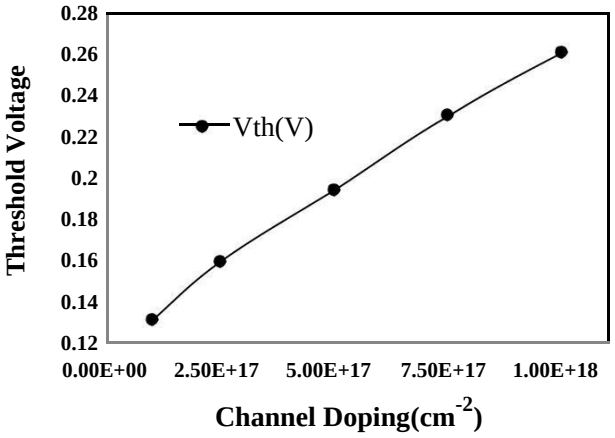

Fig. 2 Threshold voltage versus Channel Doping concentration

TABLE II
DATA FOR ON AND OFF STATE CURRENT

S.No.	Channel Doping concentration(cm^{-2})	I_{on} current (A/um)	I_{off} current (A/um)
1.	1.0x10^{17}	5.22x10^{-04}	6.06x10^{-07}
2.	2.5x10^{17}	4.79x10^{-04}	1.85x10^{-07}
3.	5.0x10^{17}	4.31x10^{-04}	4.72x10^{-08}
4.	7.5x10^{17}	3.92x10^{-04}	1.40x10^{-08}
5.	1.0x10^{18}	3.59x10^{-04}	4.38x10^{-09}

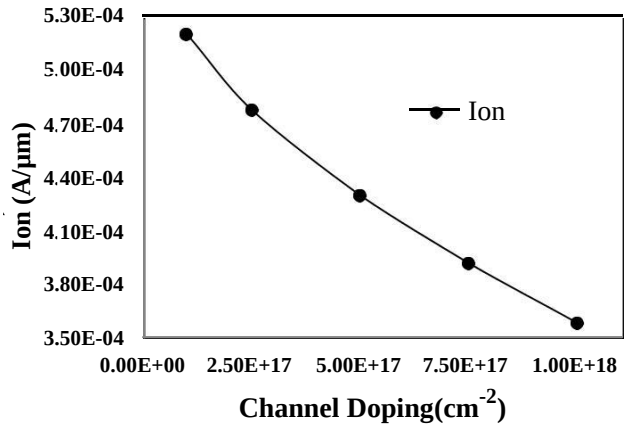

Fig. 3 I_{on} current versus Channel Doping concentration

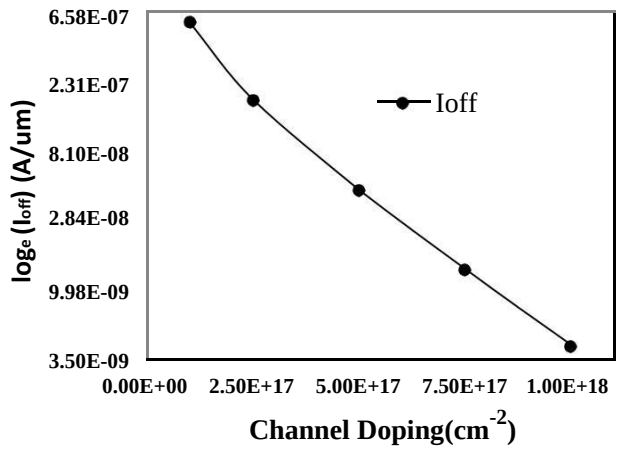

Fig. 4 I_{off} current versus Channel Doping concentration

For channel doping concentration N_{ch} < 5 x 10^{17} the off state leakage current is become a significant part. The DIBL and Subthreshold Slope (SS) are also calculated for the device for different channel doping concentration given in table III. The DIBL versus channel doping concentration is shown in Fig. 5. It is observed that DIBL is first decreasing with increasing channel doping and then increasing. The optimum value of DIBL is obtained for channel doping around 7.0x10^{17} . Similarly Fig. 6 presents the subthreshold slop which has almost decreasing nature with increasing channel doping concentration.

TABLE III
CALCULATED DIBL AND SUBTHRESHOLD SLOPE (SS)

S .No.	Channel Doping concentration(cm^{-2})	DIBL (V/V)	SS (mV/decade)
1.	$1.0x10^{17}$	.053	83.530
2.	$2.5x10^{17}$	.046	82.396
3.	$5.0x10^{17}$	.043	80.838
4.	$7.5x10^{17}$	.042	80.993
5.	$1.0x10^{18}$	.076	80.336

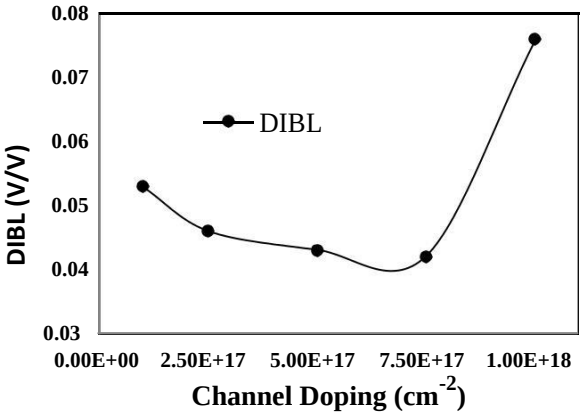

Fig. 5 DIBL versus Channel Doping concentration

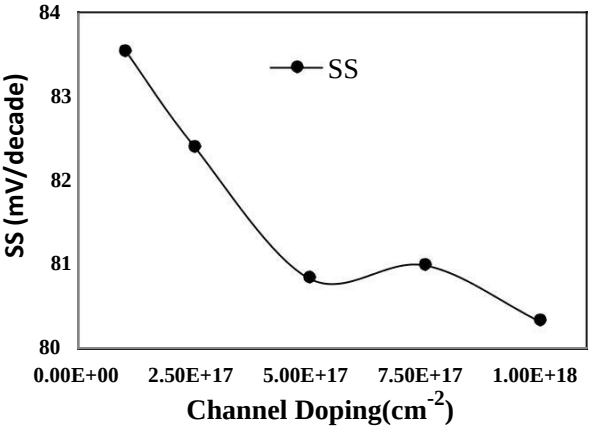

Fig. 6 Subthreshold slop versus Channel Doping concentration

IV. CONCLUSIONS

In this paper, performance optimization of a fully depleted SOI MOSFET has been carried out with the help of channel doping engineering. It is observed that threshold voltage increases with increase in channel doping concentration. I_{on} current and off state current (I_{off}) also decrease as the channel doping concentration increases. However, it is found that DIBL increased rapidly for channel doping concentration $N_{ch} > 7.5x10^{17}$. It is also well known that higher channel doping may lead to carrier mobility degradation in channel which affects the device performance. So we can vary the channel doping concentration upto certain limit.

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