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Design of Hybrid Full Adder for High-Performance Application

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***Abstract*-In this paper, a high speed, and low power full adder is proposed using a hybrid logic style. This hybrid logic structure has three modules. The first module is generated using the XOR/XNOR structure while the other two modules are realized using XOR/XNOR and CIN signal. The proposed design is simulated in the cadence software using 90nm CMOS technology. The proposed full adder design is compared with previously reported full adders in terms of delay, average power consumption and power delay product. It was found that there is 8 % and 16.75 % improvement in Delay and PDP respectively. The performance of different adders were also compared in different voltages.**

Keywords— Full Adders, Level Restorer, Cross-Coupling, High Speed, Low Power, Hybrid Logic.

I. INTRODUCTION

The explosive growth in portable devices is a leading issue in the past few years [1]. Mostly the portable devices are battery operated so power is the main concern in the VLSI system. The performance of any application-specific integrated circuits (ASIC) is restricted by its processor. ALU is a fundamental component of these processors. An Arithmetic unit performs all the arithmetic and logical operations in application-specific DSP architecture and it consumes almost one-third power of the processor. Therefore, improving the performance of the arithmetic unit, circuits can significantly increase the performance of the system [1].

In the literature [2], there are two methods to realize the arithmetic unit: the first one is the classic design style in which only one logic style is used to implement a digital design and the second one is a hybrid design style in which more than one logic style is used. In the classical approach, the Complementary metal-oxide-semiconductor (CMOS) design style uses 28-transistors to realize the full adder (FA) [2,3].

This type of adder is based on the pull-up and pull-down network. These circuits have series transistors at the output level which is a weak driver, therefore additional buffers are required for providing the necessary driving power to the next state. The advantage of this complementary CMOS style is its robustness against voltage scaling and transistor sizing. But the disadvantage is high input capacitance and requirement of buffer.

The complimentary pass transistor logic (CPL) full adder [3] with swing restoration has a dual rail structure. The advantage of one pass-transistor network (either PMOS or NMOS) is sufficient to implement the logic function. But the pass transistor logic has an inherent threshold voltage problem. Therefore, output inverters are also used to ensure drivability. CPL is not appropriate for low power application, because it has high switching activity of intermediate node, more transistor count, use of static inverters, and overloading of its input.

A transmission function full adder (TFA) [3] is made by the Transmission gate. A transmission gate is designed by connecting a PMOS and NMOS parallel to each other, and it is controlled by complementary signals at the gate of each other. The PMOS and NMOS will provide path to both 1 & 0 simultaneously. The advantage is that they have no voltage drop problem but the disadvantage is the use of a double number of the transistor for the same circuit.

Later the researchers focused on a hybrid logic style approach which uses the advantages of previously proposed logic styles to enhance the performance of the circuit. Vesterbecka proposed 14-transistor hybrid style full adder [21] having more than one type of logic. Similarly, hybrid pass-logic with static CMOS output drive full adder (HPSC) was proposed by Zhang. In this type of circuit, both XOR and XNOR are generated simultaneously. Although this Hybrid Logic style offers promising performance most of these suffer from poor driving capability.

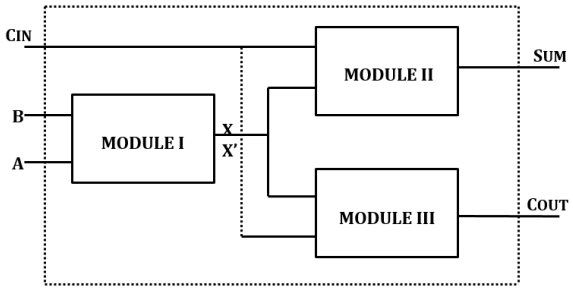


Fig. 1. Block diagram of proposed full adder

The hybrid design style based on the full adder structure has three different modules [2] [3]. Module I synthesize the intermediate signal (XOR/XNOR signals) when two input signals (A & B) are applied to it. These intermediate signals are presented with X and X' symbol in Fig1. These intermediate signals must have good driving capabilities as these signals have to drive the other two modules. Module II and Module III generate the SUM and carry outputs (COUT) respectively, using the outputs of module I and third carry input signal (CIN).

The rest of the paper is organized as follows. Section II includes the design approach of a proposed full adder. Section III includes the design approach for the XOR-XNOR module. In section IV and V, the circuit for generation of SUM and Carry out is proposed. In section VI, the circuits are simulated for power, delay and power-delay product performance and the results are analyzed for comparison.

II. HYBRID CMOS FULL ADDER DESIGN

The SUM and Carry out (COUT) expression for 1 bit FA circuit is given in the equation (1) and (2), Where A, B, and CIN are the input of FA.

$$SUM = (A \oplus B) \oplus CIN \quad (1)$$

$$COUT = A.B + CIN(A \oplus B) \quad (2)$$

In the literature Vesterbacka et.al.[4] proposed 14 T full adders. In this adder, six transistors are used to implement the module I. The other two modules (sum and carry module) are implemented using Transmission gate (TG) and 2 to 1 mux respectively. The main problem of this circuit is when inputs change from AB= 01 & 10 to AB = 11& 00, outputs reach its final voltage value in two steps. This slow response problem increases in low-voltage operation.

Another circuit of full adder which is given by Goel et.al.[2], is implemented using the 24-transistor. In this adder, a module I is implemented using CPL style and an inverter. The other two modules (module II and module III) are implemented using TG and 2 to 1 MUX respectively. But the main problem of this design is a weak driving capability. Therefore, to increase the driving capability of this circuit an inverter is used which causes an increment in power consumption.

Another structure of a hybrid adder is given by Bhattacharya et.al [3] which is implemented with 16-transistors. In this design, in module I firstly XNOR signal is generated after that XOR signal is synthesized. Module II and Module III are implemented using TG and 2 to 1 MUX.

III. PROPOSED FULL ADDER DESIGN

After reviewing the hybrid full adder designs, a new 18-transistors based FA is proposed. In this section, we explained the modules of the proposed FA.

A. Module I

The first module of FA design is the XOR-XNOR circuit, which is implemented using the cross-coupled CMOS logic and restorer circuit as shown in Fig.2. Schematic structure using PMOS and NMOS transistors is shown in Fig. 2. The choice of using cross-coupling reduces the delay and power consumption in this circuit. The 2nd topology which is level restoration provides the full swing at the output. The main key-feature of the circuit is the generation of XOR and XNOR signal at the same time rather than using an inverter to generate one output from the other. This design of XOR-XNOR provides full swing output, less delay and having small glitches, which reduces the overall power consumption of the circuit.

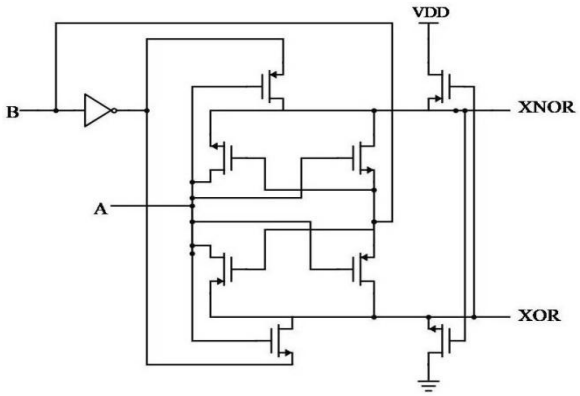


Fig. 2. Schematic structure of XOR-XNOR module

B. MODULE II

The Sum module having the four transistors is shown in Fig.3. The advantage of this arrangement is less number of transistors switching during the propagation of the signal. For some input combinations, only 1 or 2 transistors change their state which reduces its node switching activity. This

reduces the active nodes and node capacitance. Therefore by this selection of circuit, the overall delay reduces. Thus, this configuration provides less delay and less amount of power consumption for the generation of the SUM signal. No direct connection of VDD and GND in the source and drain terminal in the transistors removes the chances of short circuit current flow, which reduces the short circuit power dissipation and improves the power consumption.

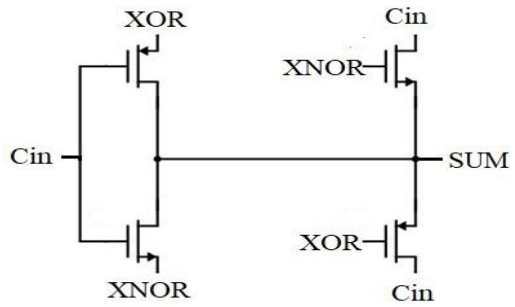


Fig. 3. Schematic structure of Sum generation module

C. MODULE III

The carry module is actually the design of the multiplexer cell as shown in Fig.4. This module is implemented using four transistors (two PMOS and two NMOS). The advantage of this circuit is the symmetrical structure, which provides less power consumption. By this structure, a minimum number of transistors will provide less area and appropriate sizing of the transistors can reduce the delay and power consumption of the circuit to the minimum extent.

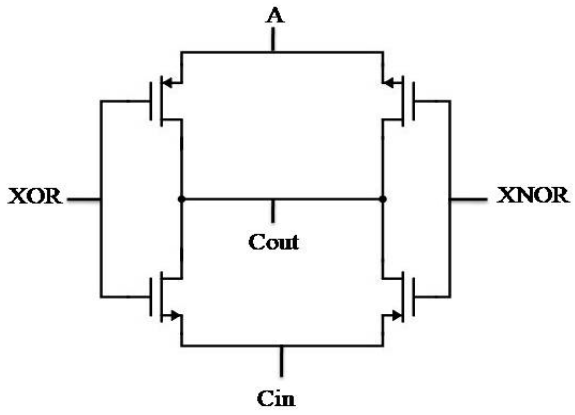


Fig. 4. Schematic structure of the carry generation module

IV. RESULT AND DISCUSSION

For the transient analysis, all the circuits have been simulated using cadence virtuoso CMOS GPDK process technology at 90 nm. Simulation results are performed with 1.2VDD and 1 GHz frequency respectively. Fig. 5 shows the transient analysis results of a proposed FA design.

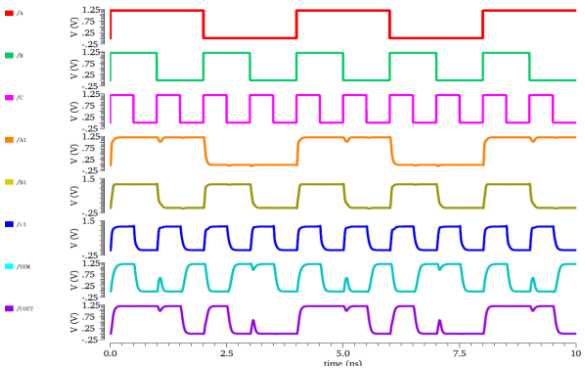


Fig. 5. Time-domain simulation results (waveform) of FA circuits

TABLE I. SIMULATION RESULTS OF DIFFERENT FULL ADDER IN 90NM TECHNOLOGY AT 1.2 V

DESIGN	Transistor Count	Delay (ps)	Power (uW)	PDP (aJ)
C-CMOS[1]	28	60.66	29.8	1807.93
CPL[1][2]	32	76.39	32.9	2513.48
TGA[2]	16	49.80	28.7	1429.37
TFA[2]	20	47.27	29.14	1377.59
14T_FA[4]	140	50.86	27.45	1396.16
FA_HYBRID_1[2]	24	67.64	28.8	1948.26
FA_HYBRID_2[3]	16	83.03	22.6	1876.61
PRO_DESIGN	18	43.11	26.6	1146.74

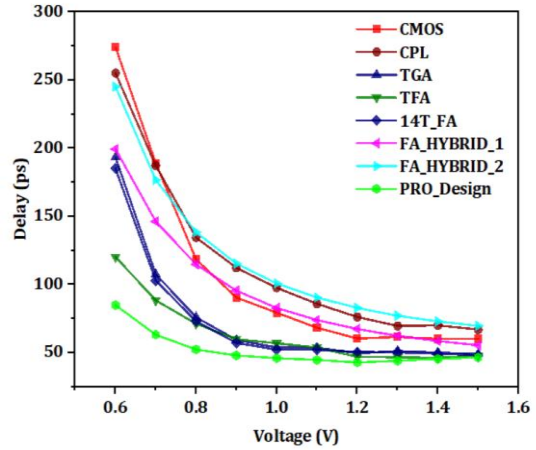
In Table I. the performance of different full adders C-CMOS, CPL, TFA, TGA, 14T_FA, FA_Hybrid_1, FA_Hybrid_2 and proposed are compared in terms of power, delay and PDP respectively.

Fig.6 presents the comparison of the performance parameter of the reviewed circuits and the proposed circuit. The delay comparison of CIN to COUT for reviewed and proposed circuit for the supply voltage 0.6V to 1.5V is displayed in Fig. 6(a). The proposed FA is 8% to 48.07% faster than other reviewed circuits.

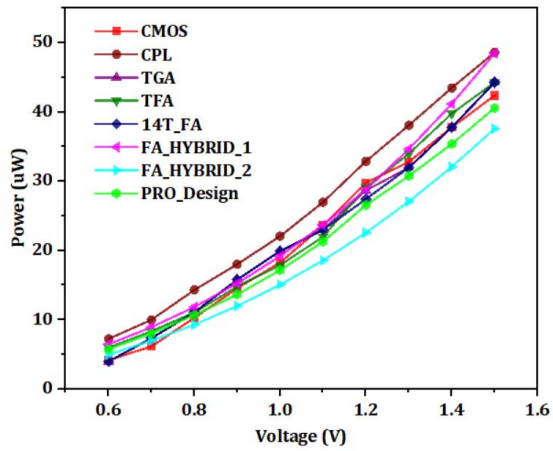
The comparison of simulation results for the proposed circuit and other reported circuits for the power consumption is presented in Fig. 6(b). It is seen from Table. I. that Bhattacharya et.al. [3] design gives minimum power because less no. of transistors are used.

The PDP for the CIN to COUT for proposed circuits and different circuits is presented in Fig. 6(c). When proposed circuit performance is compared with the

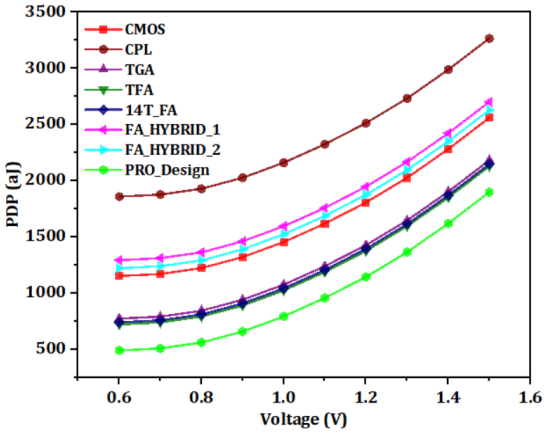
reviewed circuits the improvement in PDP was found to be 16.75% to 54.37%.



(a)



(b)



(c)

Fig. 6 (a).Delay, (b).Power and (c).PDP comparison of the different full adders for supply voltages 0.6V to 1.5V.

V. CONCLUSION

A hybrid logic full adder using level restoration and cross-coupling is proposed. The results show an 8% improvement in delay and 16.75% improvement in power delay product compared to counterparts. The proposed full adder is having only 18 transistors. The results show that the proposed adder can be a good choice for the selection of adder in case of high speed and low power circuits.

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REFERENCES

[1] A. P. Chandrakasan, S. Sheng and R. W. Brodersen, "Low-power CMOS digital design," in IEEE Journal of Solid-State Circuits, vol. 27, no. 4, pp. 473-484, April 1992.

[2] S. Goel, A. Kumar and M. A. Bayoumi, "Design of Robust, Energy-Efficient Full Adders for Deep-Submicrometer Design Using Hybrid-CMOS Logic Style," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 14, no. 12, pp. 1309-1321, Dec. 2006.

[3] P. Bhattacharyya, B. Kundu, S. Ghosh, V. Kumar and A. Dandapat, "Performance Analysis of a Low-Power High-Speed Hybrid 1-bit Full Adder Circuit," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 23, no. 10, pp. 2001-2008, Oct. 2015.

[4] M. Vesterbacka, "A 14-transistor CMOS full adder with full voltage-swing nodes," in Proc. IEEE Workshop Signal Process. Syst. (SIPS), Taipei, Taiwan, Oct. 1999, pp. 317-320.

[5] M. J. Zavarei, M. R. Baghbanmanesh, E. Kargaran, H. Nabovati, and A. Golmakani, "Design of new full adder cell using hybrid-cmos logicstyle,"18th IEEE International Conference on Electronics,Circuits, and System, pp. 451–454, 2011.

[6] M. A. Valashani and S. Mirzakuchaki, "A novel fast, low-power and high-performance xor-xnor cell," IEEE International Symposium on Circuits and Systems (ISCAS). IEEE, pp. 694–697,2016.

[7] C.-K. Tung, S.-H. Shieh, and C.-H. Cheng, "Low-power high-speed full adder for portable electronic applications," Electronics Letters, vol. 49,no. 17, pp. 1063–1064, 2013.