

# A STUDY ON TRANSCONDUCTANCE OF MICRONSCALE n-MOSFET USING HSPICE

Tejashri mane<sup>#1</sup>, Milan Sasmal<sup>\*2</sup>,

<sup>1</sup>maneteju111994@gmail.com

**Abstract**— In this paper we studied I-V characteristics of MOSFET. Then studied the graph of transconductance Vs drain current. Lastly, we investigate effect of channel length and width on transconductance. For that channel length is vary from 10um to 40um. drain voltage is taken as 5V. gate voltage varies from 1V to 4V. see the effect of channel length and width on parameter of MOSFET

**Keywords**— Drain Voltage, Drian curret, Channel length, Channel width, MOSFET, Transconductance.

## I. INTRODUCTION

One of the most important parameter for the characterization of the operation of a MOSFET is transconductance. The channel length ( $L$ ) channel widths ( $W$ ) are two important parameters for modelling and characterization of Metal Oxide Semiconductor Field Effect Transistor (MOSFET). Channel length is most important key device parameter, which is the distance between  $n^+$  - $p$  junction. Threshold voltage is nothing but the gate voltage at which an inversion layer forms at the interface between the insulating layer and the substrate of the transistor [1]. The purpose of the inversion layer's forming is to allow the flow of electrons through the gate-source junction. Therefore, threshold voltage represents the onset of significant drain current flow which also depends on channel length. In addition, threshold voltage plays an important role for the determination of device operation regimes which can be divided into three operational regions First, if the threshold voltage is less than the gate voltage ( $V_{gs}$ ), the inversion charge density is large enough to operate the device in the strong inversion region where drift current is dominant [2]. Second, if  $V_{th}$  is greater than  $V_{gs}$ , the inversion charge density is smaller than substrate doping concentration which compels the device to operate in the weak inversion region so diffusion current becomes dominant [5]. Lastly, if  $V_{th}$  is very close to  $V_{gs}$ , the inversion charge density is such that the device operates

in the transition region where both diffusion and drift currents are important. Analysis of MOSFET circuits is based on three possible operating modes: cutoff, triode (aka linear), and saturation. In cutoff, the gate-to-source voltage is not greater than the threshold voltage, and the MOSFET is inactive [4]. In triode, the gate-to-source voltage is high enough to allow current flow from drain to source, and the nature of the induced channel is such that the magnitude of the drain current is influenced by the gate-to-source voltage and the drain-to-source voltage [3]. As the drain-to-source voltage increases, the triode region transitions to the saturation region, in which drain current is (ideally) independent of drain-to-source voltage and thus influenced only by the physical characteristics of the FET and the gate-to-source voltage.

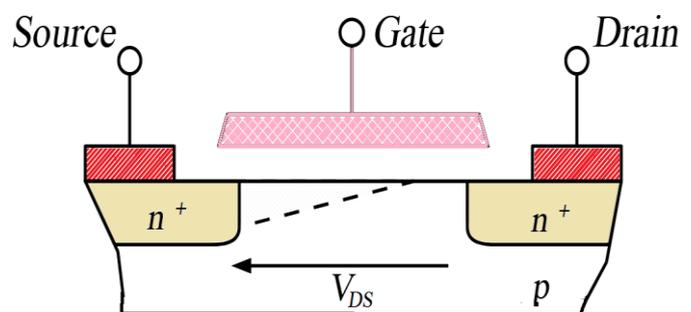


Fig.1:-Schematic representation of N channel MOSFET

Analysis of MOSFET circuits is based on three possible operating modes: cutoff, triode (aka linear), and saturation. The subthreshold region is a fourth mode, but we don't need to worry about that for this article [11]. In cutoff, the gate-to-source voltage is not greater than the threshold voltage, and the MOSFET is inactive. In triode, the gate-to-source voltage is high enough to allow current flow from drain to source, and the nature of the induced channel is such that the magnitude of the drain current is influenced by the gate-to-source voltage and the drain-to-source voltage [7-8]. As the drain-to-source voltage increases, the triode region transitions to



the saturation region, in which drain current is (ideally) independent of drain-to-source voltage and thus influenced only by the physical characteristics of the MOSFET and the gate-to-source voltage [9].

**Structure Model**

$$i_d = k_n' \frac{W}{L} (V_{GS} - V_{TH}) v_{gs}$$

$$g_m = \frac{i_d}{v_{gs}}$$

$$g_m = k_n' \frac{W}{L} (V_{GS} - V_{TH}) \dots [1]$$

Transconductance is a measure of how strong the drain current changes when the gate voltage changes. Transconductance ( $g_m$ ) is a measure of how much the drain current changes when the gate voltage changes. For MOSFET applications, the MOSFET is usually operating in the saturation region.

$$g_m \equiv \frac{\partial I_D}{\partial V_{GS}}$$

For a long-channel MOSFET:

$$g_m = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH}) \{1 + \lambda(V_{DS} - V_{D,sat})\}$$

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} \{1 + \lambda(V_{DS} - V_{D,sat})\} I_D}$$

For a short-channel MOSFET

$$g_m = v_{sat} W C_{ox} \{1 + \lambda(V_{DS} - V_{D,sat})\}$$

- gm= Transconductance
- $\mu_n$ =Surface
- Cox=Oxide thickness
- W=width
- L=length

**II. RESULTS AND DISCUSSION**

Here in this paper firstly we studied the I-V characteristics of MOSFET. In this graph we observed that when drain voltage increase drain current is increases. There is effect of drain and gate voltage on the drain current. When gate voltage increases then it show effect on the drain current also. In this graph gate

voltage is apply as 1V, 2V, 3V, 4V respectively. Drain voltage is applied as 5V. From this graph we see the effect of voltages on drain current.

Here to get the result we used the Hspice software. This is circuit simulator from that can see behaviour of circuit parameter. This is the main thing of the simulator. Origin software is also use for plotting the data. Whatever data extracted from Hspice software that plot in the origin tool. Tranconconductance is one of the most important parameter of mosfet. If the substrate is at a different voltage than the source, the threshold voltage varies due to the pn junction between source and bulk. For this lab, the source and bulk will be tied together, so this effect will be ignored.

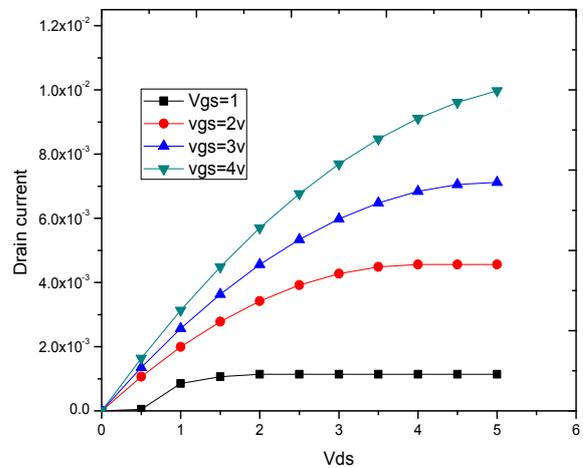


Fig.2:-ID-VDS characteristics of an n-channel MOSFET

This is the graph of transconductance Vs drain voltage. In which we can see that when drain voltage increases transconductance is also increases but after saturation region transconductance remain same there is no change in transconductance. Transconductance is a measure of how strong the drain current changes when the gate voltage changes. Here gate voltage applied from 1V, 2V, 3V 4V,5V respectively. At high drain voltage transconductance is also high. This is the relation of transconductance with the drain voltage

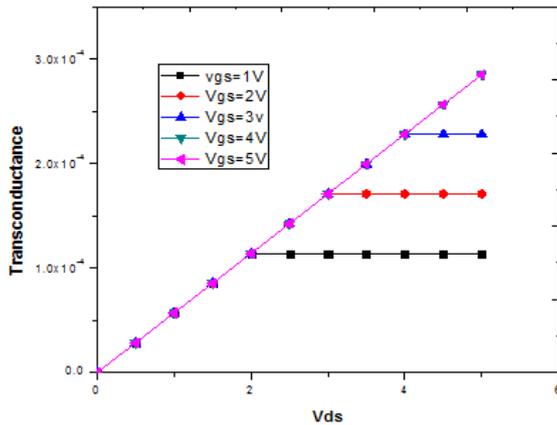


Fig 3:-GM-VDS characteristics of an n-channel MOSFET

Now the main part of the paper is see the effect of channel length and width on transconductance. In which we can see the effect of change in channel length on transconductance. For that channel length is varies from 10um to 40um and width is constant. For width is varies from 10um to 40um and channel length keep constant 60um. From the graph we see the effect of channel length and width on transconductance (gm).

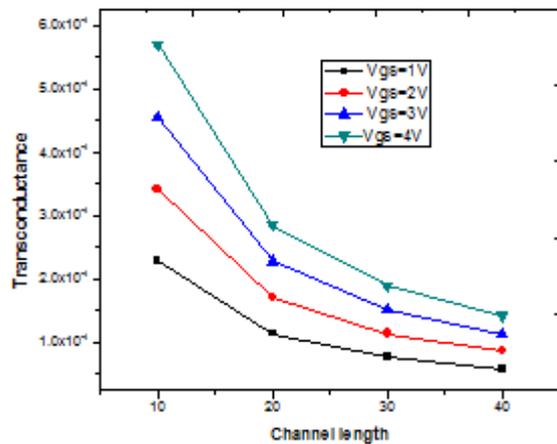


Fig 4:-Channel length Vs transconductance.

Here in this graph channel length is varies from 10um, 20um, 30um, 40um respectively. And channel width is kept constant as 60um. Gate voltage is varies from 1V, 2V, 3V, 4V respectively. Drain voltage keep constant as Vds=5V. from this we conclude that as channel length increases transconductance is decreases. Channel length is inversely proportional to the transconductance

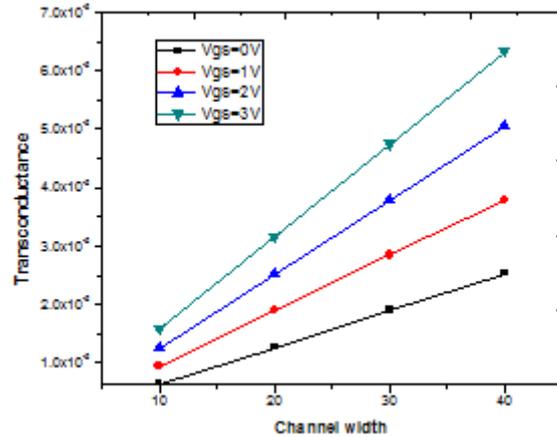


Fig 5:-Channel width Vs transconductance.

Here in this we also investigate the effect of channel width on transconductance. For this case also channel width is varies from 10um, 20um, 30um, 40um respectively. Gate voltage is also varies from 1V, 2V, 3V, 4V respectively. Drain voltage kept constant for all gate voltages. In this graph channel width transconductance increases. At minimum channel length transconductance is maximum.

### III. CONCLUSION

We investigate  $I_d$ - $V_{ds}$  characterization of Silicon n-MOSFET at room temperature by showing the effects of channel length and channel width on transconductance and investigating the effect of  $V_{gs}$  and  $V_{ds}$  also. The simulation results obtained in this work are compatible with analytical model of 1 Si n-MOS.

### IV. REFERENCES

- [1] Yuan Taur; Jianzhi Wu; Jie Min et.al Digital Circuits Transient Analysis, Parasitic, and Scalability”, IEEE Transactions On Electron Devices, Vol. 53, NO. 11, Nov-2016.
- [2] Y.M. Lin et al., High-Performance Metal Oxide Field-Effect Transistor With Tunable Polarities, IEEE Trans. on Nanotech, Vol. 4, No. 5, pp. 481-489, Dec 2015.
- [3] Aamir Ahmad, Guilherme Lawless, and Pedro Lima, Member, IEEE , EFFECT OF THRESHOLD VOLTAGE AND CHANNEL LENGTH ON DRAIN CURRENT OF SILICON N-MOSFET, May 6, 2017.
- [4] Sakurai, T., Newton, A. R. A simple MOSFET model for circuit analysis. IEEE Trans. Electron Devices, vol. 38, no. 4, pp. 887-894. June 2016.



- [5] Kwang-Sub Shin , Jae-Hoon Lee, Sang-Myeon Han, In-Hyuk Song, Min- Koo Han Elsevier Effect of channel length on the threshold voltage degradation of hydrogenated amorphous silicon TFTs due to the drain bias stress V1.10 2015-04-23.
- [6] Min-Gu Lee; Sunggu Lee, "Compact modelling for drain current of short channel MOSFETs including source/drain resistance effect" IEEE Transaction, Volume: 2 Pages: 930 - 934 vol.2,year: 2014.
- [7] QT.Morteza, Yusof1.et.al A Compact Short- Channel Model for Symmetric Double-Gate TMDFET in Subthreshold Region, IEEE Transaction on Electronic Devices Volume: 63, Issue: 6, June 2016.
- [8] Gupta, A., Mishra, D.K., Khatri, R., Chandrawat, U.B.S. and Jain, P. (2010), "A Two Stage and Three Stage CMOS OPAMP with Fast Settling, High DC Gain and Low Power Designed in 180nm Technology," in *Computer Information Systems and Industrial Management Applications (CISIM)*, 2010 International Conference on , pp. 448–453, 8-10 Oct. 2010 doi: 10.1109/CISIM.2010.5643497.
- [9] Qiang Chen , M. Harrell, James D. Meindl, "Analytical Drain Current Compact Model in the Depletion Operation Region of Short- Channel MOSFET" IEEE Transaction on electronic device, Volume: 64, Issue: 1 Pages: 66 - 72 Year: 2017.
- [10] Zhang, L., Yu, Z. and He, X. (2009), "Design and Implementation of Ultralow Current-mode Amplifier for Biosensor Applications", *IEEE Transaction on Circuits and Systems II: Express Briefs*, Vol. 56, pp. 540–544, July 2009.
- [11] Sigroha, Naveen and Krishan, Bal (2015), "A High Bandwidth Low Power Supply CMOS Operational Amplifier", *IJSRD-International Journal for Scientific Research & Development*, Vol. 3, Issue 02, 2015 | ISSN (online): 2321-0613..