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Performance and Comparison of Wallace and Vedic Multiplier

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Abstract: Speed of the multiplier depends on the hardware and algorithm used for the multiplication. A high speed multiplier reduces the computational time and is an important hardware block in digital signal processing system. Vedic multiplier is different from conventional multiplier which uses adder and shifter. This paper compares 16X16 vedicmultiplier based on UrdhvaTiryakbhyam Sutra and 16X16 Wallace multiplication. The code for the above is simulated on ModelSim.Computation of LUT value is done on Xilinx 14.5.

***Keywords*: Vedic multiplier, Wallace multiplier, Verilog, ModelSim, Xilinx**

I. INTRODUCTION

Multiplication is the process by which we multiply two numbers. A device which performs multiplication is called a multiplier. In terms of Digital Electronics a multiplier is a device which multiplies two binary numbers. Digital multiplier is the most common type of multiplier in any circuit design.Digital multipliers are important part of Digital Signal Processing Systems[1]. They are fast and reliable.They can be used to perform many operations and depending on the need of the circuit multiplier are selected.

Multipliers are extensively used in DSP applications such as convolution, FFT(Fast Fourier Transform) filtering and in microprocessors in their arithmetic and logic unit. They are also used in communication devices. In Signal and Image processing system the study and development of fast multiplier circuit has been taken up with keen interest.

Several steps of addition, subtraction and shift operations were used to implement multiplication operations. Most techniquesinvolve computing a set of partial products and then summing the partialproducts together [2]. There are various algorithm proposed which have trade off in speed,area and power consumption. Some of the multipliers are Booth multiplier, Wallace multiplier and Vedic multiplier.

Reducing power consumption and delay computation is very important requirement for many applications. Reduction in power consumption will lead to decrease in heat dissipation. Throughput and Latency are two important parametersfrom delay perspective.Throughput is the measure of how many multiplications can be performed in a given span of time.Latency on the other hand is the time required to calculate a function.

Vedic multiplier is afast and low power multiplier. A basic block of 2X2 multiplier is used as a sub block for 4X4 multiplier. A 4X4 block is used as a sub block for 8X8 multiplier and a 8X8 block is used as a sub block for 16X16 multiplier.

II. VEDIC MULTIPLIER

UrdhvaTiryakbhyam Sutra

"Vedic" originates from the word "Veda" which means a reservoir of knowledge. Vedic mathematics is a book written bySri BharatiKrsnaTirthaji[4]. The book published in 1965 describes calculation techniques based on vedas.
Vedic multiplication is divided into sixteen sutras[3]. This paper is based on the UrdhvaTiryakbhyam Sutra. The algorithm uses vertically and crosswise multiplication. As the partial products and their sum are calculated parallely the algorithm is independent of the clock frequency of the processor. Hence, it is well adapted to parallel processing. This in turn reduces delay, which is the primary aim behind this work. On comparing this algorithm to conventional multipliers this sutra has the advantage that as the number of bits increases, gate delay and area increases very slowly.This feature makes it more suitable for binary multiplications.

III. PROPOSED TECHNIQUE

A. 2X2 Vedic Multiplication

A 2X2 multiplier multiplies two numbers of 2bit each. Let the numbers be N(N_1 N_0) and M(M_1 M_0). Multiplication of the numbers is shown is equation 1.

$$\begin{array}{r} N_1\ N_0 \\ \times\ M_1\ M_0 \\ \hline N_1M_0\ \ N_0M_0 \\ N_1M_1\ \ N_0M_1 \\ \hline O_3\ \ O_2\ \ O_1\ \ O_0 \end{array} \qquad (1)$$

Figure 1: 2X2 multiplier

Firstly, the least significant bits of N and M are multiplied which gives the least significant bit of the final product O_0(vertical). Then, the LSB of the multiplicandis multiplied with the next higher bit of the multiplier and added with, the product of LSB of multiplier and next higher bit of the multiplicand (crosswise). The sum gives second bit of the final product and the carry is added with the partial product obtained by multiplying the most significant bits to give the sum and carry. Correspondingly sum becomes the third bit and carry becomes the fourth bit of the final product.The above module is known as 2X2 multiplier block.

B. 4X4 Vedic Multiplication

Now analyze a 4X4 Vedic block, say N_3N_2 N_1N_0 and $M_3M_2M_1M_0$. The output line for themultiplication result are $O_7O_6O_5O_4O_3O_2O_1O_0$.

Let's divide the number N and M into two parts, sayN_3 N_2 & N1N_0 for N and M_3M_2 & M_1M_0 for M.Using fundamental of Vedic multiplication, takingtwo bits at a time and using 2 bit multiplier block we can have the following structure for multiplication as shown in equation 2.

$$\begin{array}{l} N_3N_2\ N_1N_0 \\ X M_3M_2\ M_1M_0 \\ \hline \end{array} \qquad (2)$$

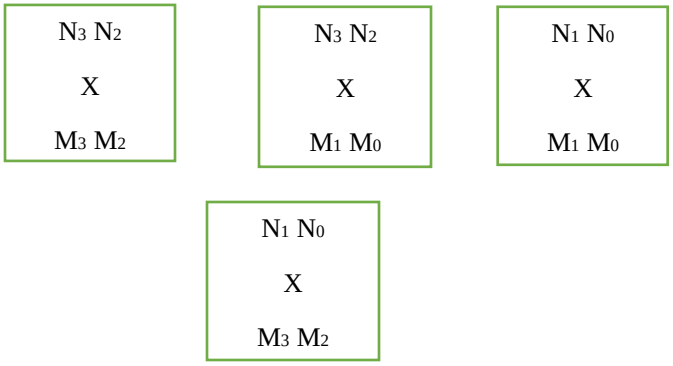

Figure 2: 4X4 multiplier

In figure 2 each block is a 2X2 bit Vedic multiplier. First 2X2 bit multiplier inputs are N_1N_0 and M_1M_0. The last block is 2X2 bit multiplier with inputs N_3 N_2 and M_3 M_2. The middle one shows two 2X2 bit multiplier with inputs N_3 N_2 & M_1M_0 and N_1N_0 & M_3 M_2. So the final result of multiplication, which is of 8 bit, O_7 $O_6O_5O_4$ O_3 O_2 O_1 O_0

C. 8X8 Vedic Multiplication

An example for 8X8 multiplication is given below. Let's say 8X8 bit multiplication of 11111111 and 00001001. We divide thenumber of bit equally and do the same analysis that used for 4X4 multiplications. It means, 11111111 will become 1111 and 1111. Similarly 00001001 will become 0000 and 1001. Hence the four different multiplications are shown in equation 3:-

(1111x0000) (1111x1001) (1111x0000) (1111x1001)

$$\begin{array}{r} 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1 \\ X\ 0\ 0\ 0\ 0\ 1\ 0\ 0\ 1 \\ \hline 0\ 0\ 0\ 0\ 0\ 0\ 0\ 0 \quad 0\ 0\ 0\ 0\ 0\ 0\ 0\ 0 \quad 1\ 0\ 0\ 0\ 0\ 1\ 1\ 1 \\ 1\ 0\ 0\ 0\ 0\ 1\ 1\ 1 \\ \hline 0\ 0\ 0\ 0 \quad 0\ 0\ 0\ 0\ 0\ 0\ 0\ 0 \quad 0\ 1\ 1\ 1 \\ 1\ 0\ 0\ 0\ 0\ 1\ 1\ 1 \\ 0\ 0\ 0\ 0\ 1\ 0\ 0\ 0 \end{array} \qquad (3)$$

Figure 3: 8X8 multiplier

In figure 3 adder will add 00000000 and 10000111 giving sum as 10000111 with no carry out, and the adder will add the result of the adders with 00001000 and will result sum as 10001111. Since no carry is generated from either of the

adder, so adder will give both sum and carry out as zero, so nothing is to be added with 0000, so final result will be: O_0=1,O_1=1,O_2=1,O_3=0,O4=1,O_5=1,O_6=1,O_7=1,O_8=0,O_9= 0,O_{10}=0,O_{11}=1, O_{12}=0,O_{13}=0,O_{14}=0,O_{15}=0.The final answer happens to be 0000100011110111.

D. 16X16 Vedic Multiplier

The design of a 16X16 block is an optimized arrangement of 8X8 blocks. The first step in the design of 16X16 block is the grouping of 8 bit (byte) of each 16 bit input. These lower and upper bytes of two inputs will form vertical and crosswise product terms. Each input byte is handled by a separate 8X8 Vedic multiplier to produce sixteen partial product rows. These partial products rows are then added in a 16-bit carry look ahead adder optimally to generate final product bits. Block diagram is shown in figure 4.

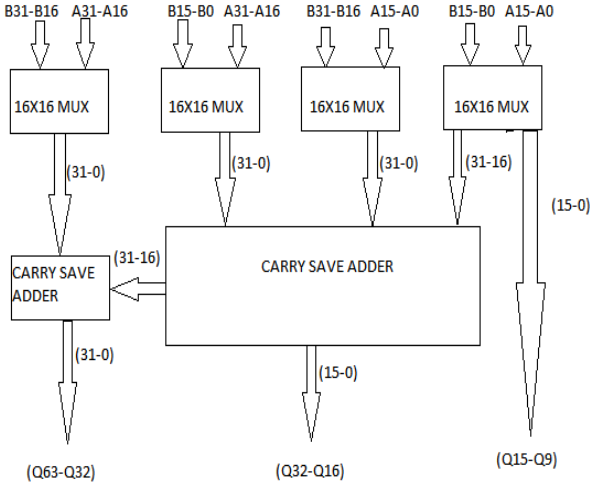

Figure 4: 16X16 multiplier

IV. WALLACE MULTIPLIER

Wallace tree is an efficient hardware algorithm that multiplies two integers, devised by Australian scientist Chris Wallace in 1964.Wallace multiplier is an efficient multiplier. Partial product array of N^2 bits are formed in the first step.In the second step, group of three rows is reduced by three 1 bit Full adders. Half adders are used for reducing two bits in a column. A single bit in a column is passed to the next stage in the same column without processing. This reduction procedure is repeated in each successive stage until only two rows are left [5]. In the final step, the remaining two rows are added using a carry propagating adder.

V. RESULT AND CONCLUSION

A. Vedic Multiplier

The output ofVedic multiplier is shown in figure 5 and figure 6.It accepts two number of 16 bits each and the result is a 32 bit number.

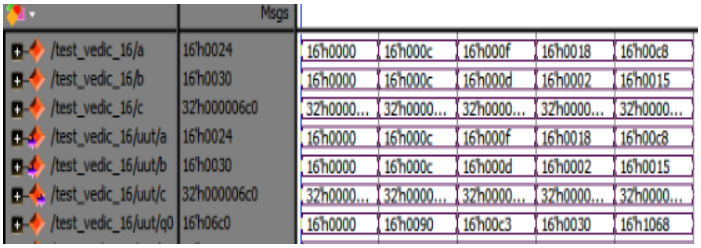

Figure 5:Output of Vedic Multiplier

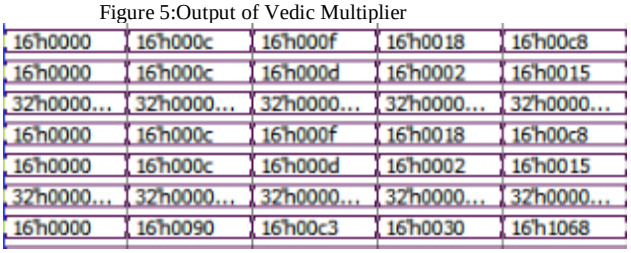

Figure 6: Outpur of Vedic Multiplier

Table I shows the number of sliced LUT used by vedic multiplier.

TABLE I :DEVICE UTILIZATION SUMMARY

Number of Slice LUTs	476	5,720	8%
Number used as logic	476	5,720	8%

B. Wallace multiplier

Output for Wallace multiplier is shown in figure 7.

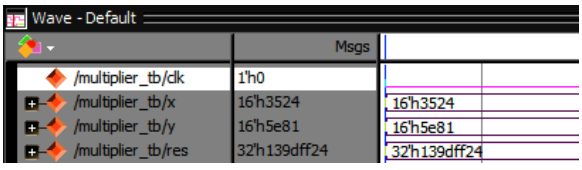

Figure 7: Output of wallace multiplier

Table II shows the number of sliced LUT used by Wallace multiplier

TABLE II : DEVICE UTILIZATION SUMMARY

Number of Slice LUTs	495	5,720	8%
Number used as logic	494	5,720	8%

Table III shows the LUT (lookup table) values for both Vedic and Wallace multiplier. The Verilog code is implemented on Spartan6E kit. The code is synthesized on Xilinx 14.5. The multiplier with more LUT value will require more transistor to run as shown in table III.

TABLE III
LUT VALUE OF VEDIC AND WALLACE MULTIPLIERS

Multiplier	LUT VALUE	KIT
Vedic	476	Spartan6E
Wallace	495	Spartan6E

Although both multiplier use 8% LUT value. Vedic multiplier has less LUT value then Wallace multiplier.

Comparing the LUT value of both the multiplier we find that Vedic multiplier will require less number of logic gates on a Spartan 6E kit.Fewer logic gates means less power is dissipated. Hence power consumption is less in Vedic multiplier.

VI. REFERNCES

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