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A Review on Quantum-dot Cellular Automata Memory Circuits

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Abstracts- CMOS technology presents some unsolved problems after shrinking certain limits. Thus for solve these problems new devices developed in place of CMOS in nanoscale era. These problems point to the need for a new kind of fundamental device and architecture, such as quantum-dot cellular automata (QCA). A QCA technology is quite different from CMOS technology. This changes the cost landscape which in turn changes the look of efficient designs. By using nanoelectronics devices like QCA it will be possible to produce high performance logic and memory integrated circuits in a small area. This paper reviewed the basics of QCA and its use in memory circuits.

Key Words-QCA, memory, clock, scaling

INTRODUCTION

Since the beginning of the seventies, the microelectronics industry has followed Moore's law, doubling processing power every 18 months. This performance increase has been obtained mainly by decreasing the size of circuit features obtained by optimization and improvement of existing technology. The current projections by the International Technology Roadmap for Semiconductors (ITRS) say that the end of the road on MOSFET scaling will arrive sometime around 2018 with a 22nm process [1]. Even getting to 22 nm presents some major unsolved hurdles. These are increasing power consumption, particularly through leakage currents, less tolerance for process variation, and increasing cost. Physical limits (quantum effects and non-deterministic behavior of small currents) and technological limits (such as power dissipation, design complexity and tunneling currents) may hinder the further progress of microelectronics on the basis of conventional circuit scaling. Quantum-dot cellular automata (QCA) is a potentially promising technology as an alternative to complementary-metal-oxide semiconductor (CMOS) technology for nanoscale device implementations.

Quantum-dot Cellular Automata (QCA) provides a new functional paradigm for information processing and communication. The main feature of this technology is the so-called processing-in-wire mechanism by which data movement and manipulation are strictly integrated. In this context, the design of memory devices is particularly challenging and interesting because the conventional storage arrangements applicable to CMOS based memories cannot be applied and innovative approaches must be used. The first section explain the basics of the QCA and then discussed some previous QCA based memory architecture and cell.

II.QCA BASICS

A lot of research has been done in the QCA devices because of its ability to go past the physical size limits of the CMOS devices [1, 2]. This includes work at circuit level as well as at device level.

Quantum-dot cellular automata (QCA) [3,4] have been proposed for implementing high performance digital circuits with low power consumption, very high density and fast operational speed [5] in nano scale era. QCA has many powerful features some of which are not available in CMOS [1][6]. Although many fabrication challenges have still to be overcome [6][7]. The simple design nature of QCA makes it attractive for investigation of new circuit topologies [8,9,10,11]. QCA topologies are not simple translations of standard circuit layouts; new ideas for translating standard logic units into QCA are needed. One of the interesting features of QCA is that there is no fixed connection strategy, and hence, it should be possible to apply optimization algorithms such as genetic algorithms to minimize the number of cells in a design.

QCA and the QCA cell was first introduced by Prof. C. S. Lent at the University of Notre Dame [3]. Quantum Dot consist of nanoscale crystals from a special class of

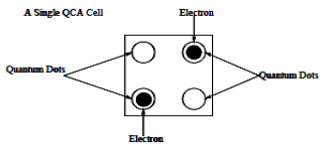

Figure 1 Single Quntum Cell

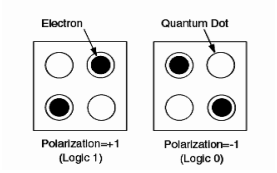

Figure 2 Representation of logic 1 and 0 in QCA Cell

semiconductor materials, which are crystals composed of chemical elements in the periodic groups II-VI, III-V, or IV-IV. The size of QD ranges from several to tens of nanometers (10¡9n) in diameter, which is about 10-100 atoms'. A QD can contain from a single electron to several thousand electrons since the size of the quantum dot is designable. QD are fabricated in semiconductor material in such a way that the free motion of the electrons is trapped in a quasi-zero

dimensional dot. Because of the strong confinement imposed in all three spatial dimensions, a QD behaves similarly to atoms and is often referred to as artificial atoms.A QCA cell as shown in Fig. 1 is considered as a square with four dot as its corners. The cell is loaded with two extra electrons (free electrons), which can quantum mechanically tunnel between cell dots but cannot tunnel between cells. With the placement of these two extra electrons in the four dots and due to the electrostatic repulsion, the two free electrons only can be at two stable positions. These two conditions considered as -1 and +1 polarity or Boolean values 0 and 1 respectively [3]. Fig.2 shows these conditions. As it was maintained, the two free electrons of each cell can only be in two stable conditions. The movement of each cell free electrons between its dots is done through tunneling mechanism. There are some barriers among adjacent dots in each QCA cell (inter-dot barriers) whose control can lead to a control of the free electrons and hence control the polarity of each QCA cell.

Various types of QCA devices can be constructed using different physical cell arrangements [8]. The fundamental QCA logic elements include a QCA wire, QCA inverter, and QCA majority gate .

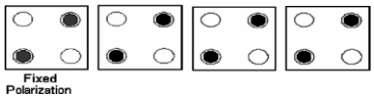

Figure 3 90 QCA Wire

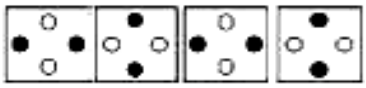

Figure 4 45 QCA Wire

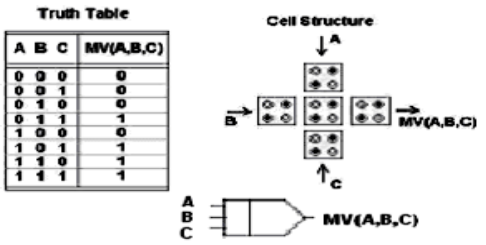

Figure 5 QCA majority Gate

In a QCA wire, the binary signal propagates from input to output because of the electrostatic interactions between cells. The propagation in a 90˚ QCA wire is shown in Fig. 3. Other than the 90˚ QCA wire, a 45˚ QCA wire can also be used. In this case, the propagation of the binary signal alternates between the two polarizations .Other QCA basic element is the majority voter (MV) with logic function MV (A,B,C) = AB + AC + BC. MV can be realized by 5 QCA cells, as shown in Figure 4. Logic AND and OR functions can be implemented from the MV by setting an input permanently to a '0' or '1' value.

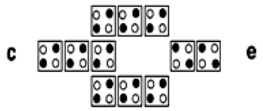

Figure 6 QCA Inverter

The inverter is the other basic gate in QCA and is shown in Figure 6. In inverter, the 45˚ displacement in the two lines of merging cells, produces complement action of the input signal. By majority voter gates and inverter It is possible to make logic circuits. Various circuits have been designed by QCA technology [10,11,12,13].

A further feature of QCA is the clocking process, clocking of QCA circuits requires a completely different approach than CMOS. A clock provides both synchronization and power gain to the QCA circuit [14]. The QCA clock is implemented by applying an E field that controls the potential barriers between quantum dots. The change in potential barriers allows to control the rate at which the electrons quantum mechanically tunnel between the dots in the QCA cell and therefore, the switching of its polarization. When the clock signal (through the E field) is low, the potential barriers between dots are low because no polarization exists.

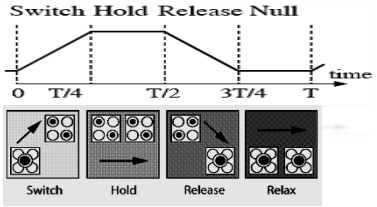

Figure 7 Clocking process in QCA

Clocking in QCA [14] is implemented as follows: the QCA circuit layout is divided in adjacent zones that pertain to the four phases of the clock. Each of the clock signals is shifted by 90 degrees from the previous one as shown in Fig. 7. The slope of the transitions must be sufficiently small to maintain the cells near the ground state. This technique (known as quasi-adiabatic switching) has been proposed in [14]. In the first phase, the clock signal rises (the switch state) and the polarization of the cell is dependent on the neighboring cells. In the second phase (the hold state), the clock signal remains high, thus preventing the tunneling of the electron pair and therefore, latching the information inside the cell. In this phase, the information can be used as input to the neighboring cells that are in the switch state. In the third phase (the release state), the clock signal is lowered and the cell becomes unpolarised. In the last phase (the relax state), the clock signal is kept low and the cell stays unpolarised.

III. QCA MEMORY CIRCUITS OVERVIEW

When transistors are scaled down in size, many problems arise to in memory circuits. First the leakage current increases. Leakage current translates to heat generation which limits the density of storage. If memory cells are too close together, the

heat generated could destabilize the cells. This constraint will limits the density of CMOS memory at the nanoscale. Memory array architecture does not translate well to the nanoscale due to an increase in both transient and permanent errors. Transient faults will be more common because the energies at which bits are stored will be lower than current memories and will therefore be more susceptible to fluctuations due to doping problems both at fabrication time and caused by electro migration of atoms during memory operation. Permanent errors will also be more common because of the difficulty of fabrication at the nanoscale. Memory design in QCA present unique characteristics due to their clocking structure. Since memory is one of the most applicable basic units in digital circuits, having a fast and optimized QCA- based memory cell is remarkable. Various works have been done in the memory architectures based on QCA.

In the technical literature, QCA based memories can be mainly classified into parallel and serial architectures. A parallel architecture offers the advantage of low latency, at each memory cell, only one data bit is stored, so there is no delay in that bit reaching the Read/Write circuitry. In a serial design, multiple bits are stored in each memory cell and share the Read/Write circuitry, thus resulting in a delay proportional to the word size. [15] has made an early attempt to design a serial QCA memory using the so-called **SQUARES formalism.** The basic principle of this technique is to define a set of equally sized blocks, each performing a basic function in QCA. These blocks can then be tiled together to design more complex QCA circuits. The obvious advantage of this technique is the ease in the geometric layout. However, as the blocks are of standard size, a substantial unutilized area appears in each block, thus causing spatial redundancy and lower density in the overall design. Clocking each SQUARE requires a large number of clocking zones even for a modest memory size, thus also requiring a considerable amount of CMOS circuitry to generate the clocking signals. [16] has introduced a **H-Memory architecture** with high density and uniform access time. The H-Memory has a complete binary tree structure with control circuitry at each node; as the memory spirals are at the leaf nodes, an integration of logic and memory is accomplished in the layout, but the control circuitry and memory are logically separate (similarly to CMOS design). However unlike conventional designs, control and data bits are serialized. The bit stream enters the memory structure at the root node and traverses down the tree by utilizing one control bit for routing at every node in the path. The architectural choice of dealing with serial bit streams results also in rather complex control logic for QCA. The memory cell at each leaf node is a spiral allowing storage of several bits, while sharing clocking zones between multiple loops. In this design, the memory size at each spiral and the cell count do not have a linear relationship; each outer loop has an increasing diameter, thus requiring more QCA cells for its implementation (although its storage capacity remains constant). [17] has proposed a **conventional parallel memory architecture** (such as encountered in CMOS-based RAM design) for QCA, i.e. by storing one bit at each memory cell. The single-bit memory cells allow the design of a simple Read/Write circuitry; each memory cell is implemented using 170 QCA cells and the select signals are separately generated using decoders. The main disadvantage of this approach is the same as the one encountered in [15] namely, data in each memory cell is stored using a closed QCA wire loop (which is partitioned into four clocking zones). Also, clocking zones cannot be shared between memory loops and their dimensions are very small. Therefore, the memory design requires a large number of clocking zones, thus complicating the routing of underlying clock lines. The **hybrid memory architecture** [18] combines the advantages of reduced area of a serial memory with the reduced latency in read operation of a parallel memory, hence its name the hybrid. This architecture is best suited in applications in which data is written rarely or in a burst mode, but the read operation is performed often (e.g. like the program memory of a microprocessor).

There are two common type of memory cell in QCA: Loop based memory cell and Line based memory cell. The popular loop based memory cell proposed in [15] stores data bits circulating on the feedback loop (Fig 9) of QCA cells. The feedback is processed within four clocking zones. These four clocking zones are generated by the conventional four phases of clocking strategy, as illustrated in Fig. 10, thus no additional clock generators are necessary. Furthermore, the read/write circuitry can be quite complex for serial access memories. Above mentioned all architecture used the loop based memory cell.

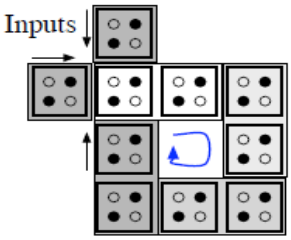

Figure 8 Loop based memory cell

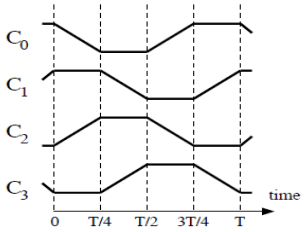

Figure 9 Conventional four phase clocking

The line based memory cell stores data bits propagating back and forward on a line of QCA cells. The **Line Based Memory[19]** is a novel logic arrangement for the MV, namely the wires to an MV can behave differently (either as input or output) in time depending on the clock phase in which they are operative. This arrangement combined with a new clocking strategy, overcomes the limitation of a traditional unidirectional flow of logic signals in QCA.The

line-based memory design in [20] uses three clock zones (in addition to the four clock zones on the rest of the circuit) as shown in Fig.11. [20] purposed the parallel memory architecture using the line based memory cell. This architecture requires two additional clocking signals as the line based operation of the memory cell needs three zones and four step process whose timing is different from the commonly used for adiabatic switching.

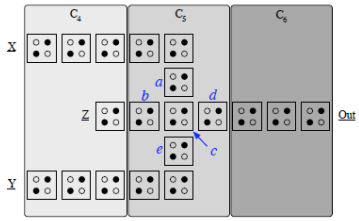

Figure 8 Line based memory cell

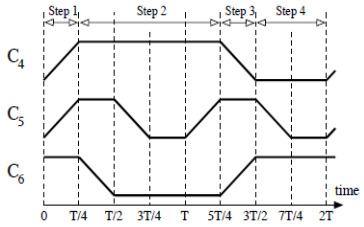

Figure 9 Three phase clocking scheme for the line memory

The line based parallel memory design proposed in [21] requires an easy-to-implement, dual-phase clocking scheme. Dual-phase clocking is implemented with two clock phases which have the same duty cycle and are phase-shifted by half a clock cycle, thus, requiring only one additional clock generator. Hence this reduces the number of QCA cells and clocking zones of the three-phase implementation presented in [20]. A Line based serial memory architecture [22, 23] consists of two long horizontal wires connected together at both ends by two short verticals wire, thus creating a loop for memory in paradigm. Thus in this architecture utilizes new building block (called tiles) in the storage and input output circuitry. Clocking zones are shared between memory cells and length of QCA line of a clocking zone is independent of the word size.

The main advantage of the line-based approach is that the clocking distribution circuitry is dramatically simplified because the same clocking zones can be shared by different memory cells. In brief, compared to the loop-based memory cell, line-based memory cells are much simpler in that line based memory cells can be stacked into a matrix structure. Also, the density of the line-based memory is higher than the loop-based memory cell, as the unused space inside the feedback loop affects utilization.

However,peripheral Read/Write circuits of these architectures [22, 23] are complex, clock circuitries and the entire memory cell are still difficult to fabricate despite the improvement compared to loop-based core. Clock zones do not have a clear and regular partition. Moreover, these two kinds of memory cell cost many cells, control cells and layout areas. Thus the improves memory cell [24] that exploits regular clock zone by employing two new clocking signals and a compact Read/Write circuit. The clock circuitry is very regular, helping manufacturability for physical implementation.

[25] proposed a more efficient memory design around line based memory introducing parallel read. The proposed supporting logic enables realization of such a high speed memory system. Its power to execute simultaneous read write operation is exploited in designing digital signal processors.

[26] purposed improved loop-based Random Access Memory (RAM) cell. In this the inherent capabilities of QCA, such as the programmability of majority gate and the clocking mechanism have been considered. The wasted area has been reduced compared to traditional loop-based RAM cell and the memory access time has been duplicated in presence of smaller number of cells. In [27] memory cell with set/ reset ability will be introduced. This designs have a simple and robust structure and do not need any crossover wire.

IV. CONCLUSION

Nanoelectronics, including quantum-dot cellular automata, focuses on the integration of molecule sized elements. By joining these elements in specific patterns, engineers and scientists have the potential to create a new generation of logic and digital capabilities far beyond what Moore's Law projected for transistors some 30 years ago. There are many challenges to overcome before quantum dots will affect society on a daily basis, including temperature requirements and the feasibility of mass production. Yet, working together in multidisciplinary teams, researchers can and will find a way to make circuits smaller, faster, and better.After review the QCA and QCA Memory Architecture previous work still there are many limitations. The following issues in QCA memory Circuits design:

- Provide a regular and simple clock zone which help manufacturability for physical implementation.
- Provide compact Read/Write signal
- Remove waste area in memory cell.
- Sharing the clock zone.
- Synchronization in memory cell clock and other memory circuits for proper operation.
- Increase in memory capacity.

Nanoscience offers new frontiers in engineering devices on a molecular level that are well on their way to us hering electronics into the next century.

Thus the design of QCA memory cell and memory architecture calls further improvement for getting high density , high speed , less power ,high performance and larger memory word.

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