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Comparative Analysis of Nano-Scaled Low Power 10t Sram Cell At Various Technology Nodes

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Abstract— In this paper, the study of 10T SRAM Cells which has been one of the versatile circuits in digital circuit design. The variation of parameters like Power dissipation and Total propagation delay with respect to Vdd and temperature has been analysed in 45nm, 65nm and 90nm technology. TANNER EDA simulation tool has been used for simulation of various parameters of SRAM Cells. In this work, graphs have been drawn for power dissipation and delay in all operations of the cells.

***Keywords*— VLSI, VDD, SRAM, SPICE, RWM, Delay, Power, Temperature**

I. INTRODUCTION

V*ery Large*-**S***cale* **I***ntegration* is the process of placing thousands (or hundreds of thousands) of electronic components on a single chip. Nearly all modern chips employ VLSI architectures, or ULSI (ultra large scale integration). An SRAM (Static Random Access Memory) is designed to fill two needs: to provide a direct interface with the CPU at speeds not attainable by DRAMs and to replace DRAMs in systems that require very low power consumption [3]. In the first role, the SRAM serves as cache memory, interfacing between DRAMs and the CPU. Figure 1 shows a typical PC microprocessor memory configuration.

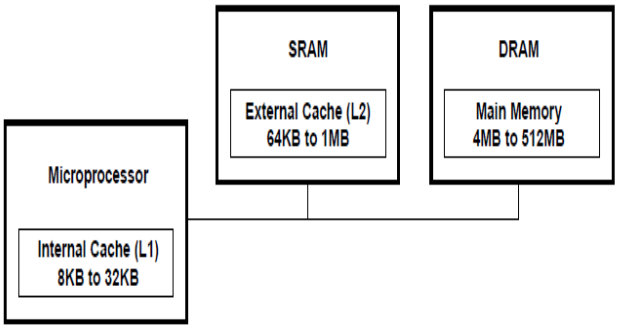

Figure 1 Typical PC microprocessor memory Configuration

Fast low power SRAMs have become a critical component of many VLSI chips. This is especially true for microprocessors, where the on-chip cache sizes are growing with each generation to bridge the increasing divergence in the speeds of the processor and the main memory. Simultaneously, power dissipation has become an important consideration both due to the increased integration and operating speeds, as well as due to the explosive growth of battery operated appliances [5].

10T SRAM CELL

Figure 2 shows the schematic of the 10T sub threshold bit cell. Transistors are identical to a 6T bit cell except that the source of M1 and M2 tie to a virtual supply voltage Vdd.

Cell Structure

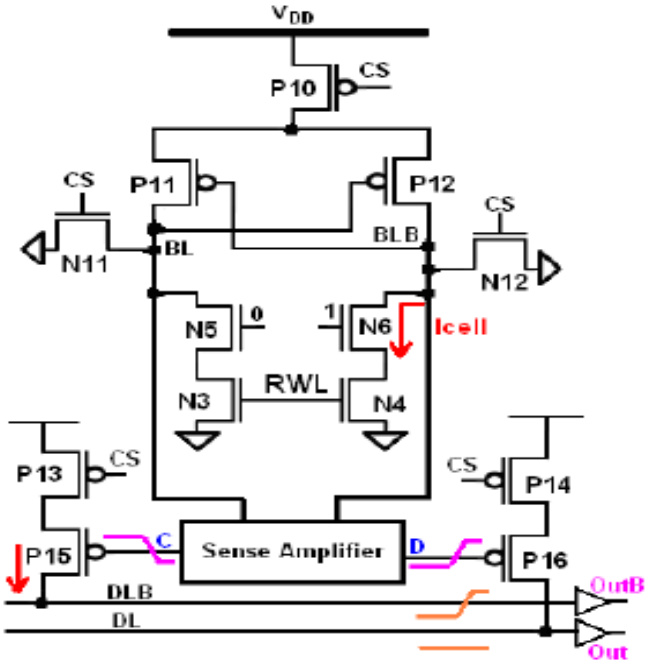

Figure 2 10T SRAM Cell

Figure2 shows the schematic of the proposed cell with separate read and writes ports. It consists of four p-MOS (P1–P4) and six n-MOS (N1–N6). Like the conventional SRAM, P1, N1 and P2, N2 form a cross-coupled inverters flip-flop

which has two stable states to store either a '0' or a '1'. Figure2 illustrates a simplified read data path of the proposed design with two BL pre-charge transistors (N11, N12), pull-up transistors (P10-P12), a bit line sense amplifier and four data lines driving transistors (P13-P16). During standby, both BLs are pre-charged to ground, as shown in Figure 2. When a read operation is activated, a specific memory cell is chosen by its corresponding Read Word Line (RWL) and Column Select (CS) signals (Figure2). Consequently, N11 and N12 are turned off to release the BLs. As P10-P13 is turned on, they charge the BLs up from ground level. From now on, for the ease of explanation, assuming that the chosen cell stores a '0', N5 is off whereas N6 is ON. Since RWL is trigger high, a small current I_{cell} flows from BLB to ground, causing VBLB to rise slower than VBL, i.e. VBLB < VBL. Thus, VGS of P11 is larger than that of P12 and P11 sources a higher current than P12. Consequently, VBL continues to rise with a higher rate than VBLB and quickly creates a large voltage gap between these two lines. A simple buffer is then used to provide full CMOS logic level outputs. Although the RWL signal turns on N3 and N4 of all the cells in the same row, the BLs of the other column are kept at ground level and hence no I_{cell} flows into the other cells on the accessed row. Thus, power dissipated within the SRAM core is mainly consumed by the sense amplifier and an amount of current is saved. The proposed SRAM design has a similar write operation as the conventional design. When data is transferred to the BLs, the Write Word Line (WWL) turns on the access transistors of the cells and data is written. However, since the precharge level of BLs is ground, p-MOS transistors (P3 and P4) are used to access the memory instead of n-MOS transistors (N3 and N4). This results in a slightly smaller cell current during a write and hence the proposed design has a slower write delay and a lower write power when compared to the conventional 6T design. The proposed design has 24% layout area overhead when compared to the conventional 6T layout due to four additional n-MOS transistors and the wiring of the additional RWL. However, as technology scales down, excessive fabrication fluctuations require 6T design to use larger transistor size to maintain its stability [10]. Thus, the 10T design has its advantage as the area overhead can be reduced when minimum size transistors can be used while maintaining its high stability.

Read Operation

Read access is a single ended and occurs on a separate bit line, RWL, which is precharged to prior to read access. The word line for read also is distinct from the write word line. One key advantage to separating the read and write word lines and bit lines is that memory using this bit cell can have distinct read and write ports.

Write Operation

Write access to the bit cell occurs through the write access transistors, M5 and M6, transistors from the write bit lines, WBLT and WBLC. Transistors M8 through M10 implement a buffer used for reading.

II. CIRCUIT DIAGRAM

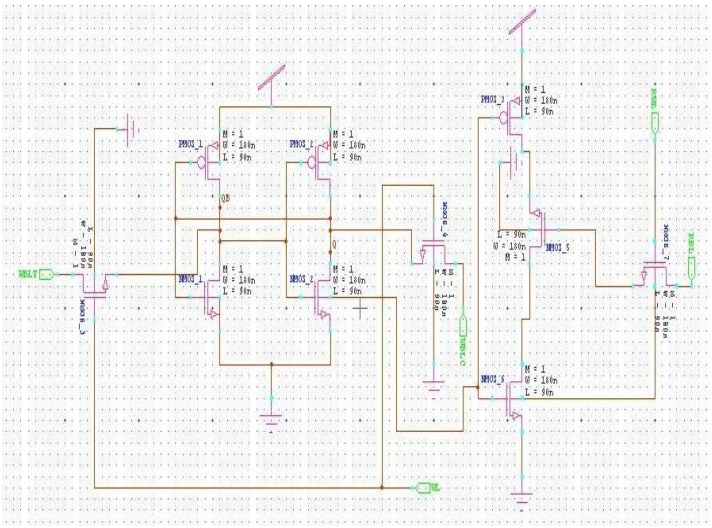

Figure 3 Schematic of 10T SRAM

In this schematic, the 3 PMOS and 7 NMOS transistors are used. The length and width of these are to be set like length is equal to the technology and width is double to the length. In this, the input terminals WL, RBL is equal to 1 and RWL is equal to idle voltage 1.1, WBLT and WBLC is complimentary to each other. And the Output terminals Q and QB obtained complimentary to each other corresponding to WBLT and WBLC. Simulation is done on three technologies 45nm, 65nm and 90nm. And calculate the power dissipation and Delay with the variations of Vdd and Temperature.

III. SIMULATION & RESULTS

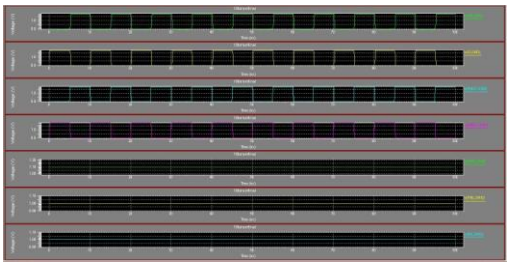

Figure 4 W-EDIT Waveform

Effect of variation of Vdd on power

In 10T SRAM cell, the average power dissipation is calculated with the variations of Vdd from 1.2V to 1.8V at 45nm, 65nm and 90nm technology and the least power dissipation has been observed at 45nm technology with 1.2V Vdd which is 0.01µW.

Technology	45nm	65nm	90nm
Vdd(V)	POWER (µW)	POWER (µW)	POWER (µW)
1.2	**0.01**	22.60	13.15
1.4	0.023	33.1	22.1
1.6	0.063	52.8	35.7
1.8	0.209	67.75	58.7

Table 1 Power with the variation of Vdd

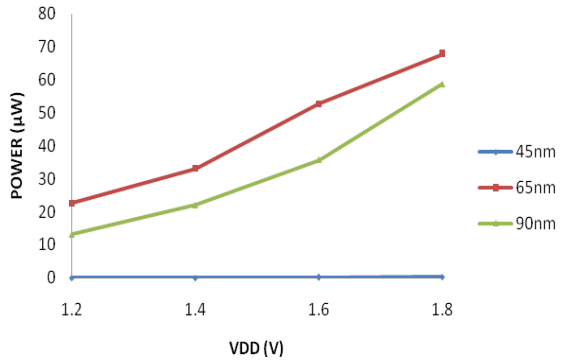

Figure 5 Variation of power with respect to Vdd

Effect of variation of Vdd on Delay

In 10T SRAM cell, the total propagation delay is calculated with the variations of Vdd from 1.2V to 1.8V at 45nm, 65nm and 90nm technology and the least delay has been observed at 45nm technology with 1.8V Vdd which is 47.6ps.

Technology	45nm	65nm	90nm
Vdd(V)	DELAY (ps)	DELAY (ps)	DELAY (ps)
1.2	66.6	77.5	72.4
1.4	59.1	71.7	67.9
1.6	54.8	63.5	64.4
1.8	**47.6**	64.1	64.1

Table 2 Delay with the variation of Vdd

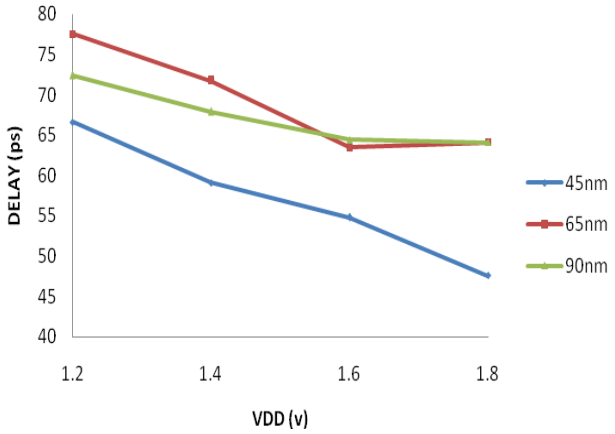

Figure 6 Variation of Delay with respect to Vdd

Effect of Variation of Temperature on Power

Technology	45nm	65nm	90nm
TEMP(^{0}C)	POWER (µW)	POWER (µW)	POWER (µW)
100	0.368	13.7	11.26
200	0.807	6.29	4.92
300	7.549	22.4	26.63

Table 3 Power with the variation of Temperature

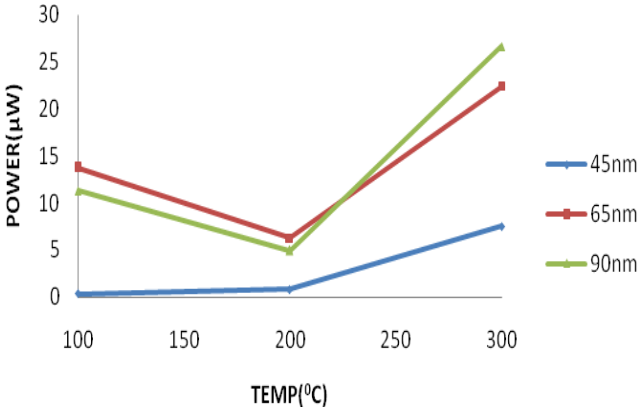

Figure 7 Variation of Power with respect to Temperature

Effect of Variation of Temperature on Delay

Technology	45nm	65nm	90nm
TEMP(^{0}C)	DELAY(ps)	DELAY(ps)	DELAY(ps)
100	93.87	163	127
200	80.72	169	125
300	75.49	152	112

Table 4 Delay with the variation of Temperature

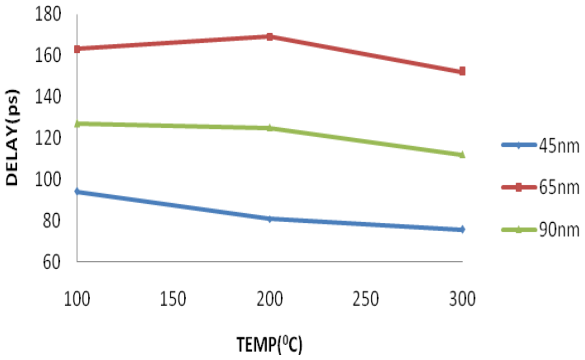

Figure 8 Variation of Delay with respect to Temperature

IV CONCLUSION AND DISCUSSION

Simulation of memory cells has been performed in TANNER EDA (14.11v). In simulation work, operations were analyzed through waveforms and output files obtained. Power and Delay are the important factors calculated in this work. First factor is power. Second performance factor is delay. Delay determines speed of memory cell for reading or writing the data. Delay has been obtained by reading the waveforms time duration after which the data becomes stable at a particular voltage level that may be logic '0' or logic '1' In case of 10T SRAM cell, Least Power (0.01µW) shows at 45nm technology at Vdd 1.2v. Whereas least Delay (47.6ps) shows at 45nm technology at Vdd 1.8v. The 10T Sram has less power dissipation in comparison with 6T Sram because it has different read and write operations.

REFERENCES

[1] Neil H.E.Weste, David Harris and Ayan Banerjee "CMOS VLSI DESIGN – A Circuits and System Perspective" Pearson eduction, Third edition, ninth impression 2009, pp. 385.
[2] Integrated Circuit Engineering Corporation "Sram Technology" pp. 8.10-8.11
[3] WIKIPEDIA" Static Random access memory" http://en.wikipedia.org/wiki/Static_random_access_memory, 2009
[4] Sung-Mo Kang, Yusuf Leblebici "CMOS Digital Integrated Circuits Analysis and design" TATA McGRAW-HILL, Third Edition.
[5] Neil H.E.Weste, David Harris and Ayan Banerjee "CMOS VLSI DESIGN – A Circuits and System perspective" Pearson eduction, Third edition, ninth impression 2009, pp. 179.
[6] Yu Cao, Dejan Markovic and Jan Rabaey "SRAM Leakage Suppression by Minimizing Standby Supply Voltage" IEEE computer society, 2004Ethan H. Cannon, Daniel D. Reinhardt and Paul S "SRAM Ser in 90, 130 And 180 nm bulk" IEEE 04CH37533 42 Annual International Reliability Physics Symposium. Phoenix.
[7] Shigeki Ohbayashi, Makoto Yabuuchi, Koji Nii and, Susumu Imaoka "A 65-nm SoC Embedded 6T-SRAM Designed for Manufacturability With Read and Write Operation Stabilizing Circuits" IEEE journal of solid-state circuits, Vol. 42, April 2007, pp 820 -829
[8] Eiji Morifuji, Dinesh Patil, Mark Horowitz, oshio Nishi" Power Optimization for SRAM and Its Scaling" IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 54, NO. 4, APRIL 2007
[9] Abhijit Sil, Soumik Ghosh, Neeharika Gogineni, Magdy Bayoumi" A Novel High Write Speed, Low Power, Read-SNM-Free 6T SRAM Cell" 978-1-4244-2167-1/08/$25.00 ©2008 IEEE
[10] Sapna Singh, Neha Arora, Prof. B.P. Singh" Simulation and Analysis of SRAM Cell Structures at 90nm Technology" International Journal of Modern Engineering Research (IJMER), Vol.1, Issue.2, pp-327-331 ISSN: 2249-6645